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## SUBSTITUTE SPECIFICATION

### GROUND PLANE FOR A SEMICONDUCTOR CHIP

#### BACKGROUND OF THE INVENTION

##### Field of the Invention

[0001] The present invention relates to the design and production of integrated circuits and to the packaging of such circuits, more specifically the invention relates to a ground plane for a semiconductor chip for mounting on a supporting member in a chip package.

##### Description of the Prior Art

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[0002] In all analog circuit designs it is desirable to have a ground that is as close to 0 volt AC as possible. Normally circuit design assumes that ground nodes do not carry any AC-voltage. If a ground node, contrary to this assumption, does carry an AC-voltage, this may lead to unpredictable behavior, e.g. increased noise, distortion or even instability. The root cause of this is that all conductors have a non-zero impedance. This means that when a ground node has to source or sink a current there will be a voltage drop between the ground node and the actual ground point. This effect is much more pronounced in RF-circuits because the inductive nature of the impedance.

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[0003] In integrated circuits the ground point of the die (semiconductor chip) is connected to the exterior via a bonding wire connected between the die and the interposer (or leadframe). The impedance of the bonding wire is important at RF-frequencies, and this makes it difficult to realize proper ground node on the die. If the die is made bigger in order to make the bonding wire shorter, this only moves the problem from the bonding wire to the die because the conductor on the die has to be longer.

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[0004] Several solutions have been proposed to solve this problem. One is to make the C-package very small and the bonding wires short. This solution has several drawbacks. It is only viable for small scale integration circuits. In large scale integration circuits the die is larger and the ground conductors on the die are correspondingly longer. And even for small scale integrated circuits making the bonding wires short only reduces the problem, but does not solve it.

[0005] Another solution is to have multiple conductors in parallel. This is often used in RF-PA-stages, but is not really practical for large scale integrated circuits as the multiple connections take up a lot of space

#### SUMMARY OF THE INVENTION

[0006] According to a first aspect of the invention, an AC-ground plane is provided for a semiconductor chip for mounting on a supporting member in a chip package, wherein the ground plane comprises at least one first capacitor plate provided within the chip, and at least one second capacitor plate provided on the supporting member, the first and second capacitor plate being separated by a

dielectric layer and capacitively coupled to each other via this layer, and the ground plane comprising at least one first conducting member, the first conducting member being at least one electrically conducting via extending through the supporting member and electrically coupled in series with the second capacitor plate.

**[0007]** According to a second aspect of the invention, an AC-ground plane is provided for a semiconductor chip for mounting on a supporting member in a chip package, comprising a capacitor and an inductor having a resonant frequency which approximately equals the working frequency of the integrated circuit.

**[0008]** A third aspect of the invention is a method for providing a tuned RF-ground plane for a semiconductor chip mounted on a supporting member in a chip package. The method includes steps of providing a metal covered area on the surface of the supporting member, and providing a number of vias electrically connected to the metal covered area and extending therefrom through the supporting member to the opposite side thereof, connecting in parallel at least two of the number of vias.

**[0009]** In general terms according to the present invention the problem is solved by placing a metal-covered area on the interposer under the die. Vias on the interposer connect the area to the underside of the interposer. The die is glued to the area with conducting glue. A capacitor is thus formed, the capacitor being formed by the die substrate, the oxide layer on the underside of the die, and the conductive plate on the interposer. By making all other associated impedances as small as possible, e.g. by connecting the metal-plate on the top side of the interposer to the bottom side by using multiple vias in parallel, the

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resulting impedance can be made very low, less than 20 Ohms, even at high frequencies. If the integrated circuit has a well defined working frequency, the RF-ground plane can be tuned to that frequency by choosing the dimensions of the associated conductors, and thus the inductance of the conductors, so that the resonant frequency of the inductance and capacitor coincides with the working frequency. The impedance at said working frequency can be made extremely low, close to 2 Ohms.

**[0010]** According to a third aspect of the invention, there is provided a semiconductor chip package comprising a semiconductor chip and a supporting member, the supporting member comprising at least one metal covered area and at least one electrically conductive via extending from the metal covered area through the supporting member. The semiconductor chip package is attached to the supporting member by means of conductive glue which is in electrical contact with the metal covered area.

**[0011]** The invention will now be described in more detail, by means of the drawings, which show non-limiting exemplary embodiments of the invention.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0012]** Fig. 1 schematically shows a cross section of the preferred embodiment of a semiconductor chip and interposer assembly of an integrated circuit package according to the invention in a situation where the assembly is mounted on a printed circuit board (PCB).

**[0013]** Fig. 2 shows a top plan view of the chip and interposer assembly of Fig. 1.

**[0014]** Fig. 3 schematically shows an electric circuit diagram for the LC series circuit of the chip and interposer assembly of Fig. 1.

**[0015]** Fig. 4 schematically shows impedance characteristics for the bonding wire and via, and the total impedance, respectively, for the preferred embodiment.

#### DETAILED DESCRIPTION OF THE INVENTION

**[0016]** Referring first to Fig 1, there is shown a semiconductor chip 1. The semiconductor chip includes an insulating layer 2. Typically this layer 2 is an integrally formed layer comprising an oxide of the semiconductor material, i.e. silicon dioxide if the chip is made from silicon. The dielectric coefficient of silicon dioxide is approximately 3.9.

**[0017]** The chip 1 is glued to an insulating interposer 4 carrying a conductive area 5. Typically the conductive area 5 is a metal covered area. The glue 3 is conductive and serves not only the purpose of adhering the chip 1 to the interposer 4, but also forms a capacitor plate, capacitively coupled to internal parts (not shown) of the chip, but insulated therefrom by the insulating layer 2.

**[0018]** In the following these internal parts are referred to as capacitor plates regardless of their actual shape, i.e. all current carrying parts within the chip are considered as forming capacitor plates.

**[0019]** From the conductive area 5 on the surface of the interposer 4 a number of vias 7 extend through the interposer 4 to the opposite surface thereof, where they contact a printed circuit board (PCB) 10.

**[0020]** In this respect it should be noted that even though the metal coated area in the embodiments shown corresponds largely to the dimensions of the chip

this is not a prerequisite for the invention to work. Instead, because the conductive glue defines the capacitor plate vis-à-vis the internal parts, it is in principle sufficient to contact the glue 3 to the vias 7.

[0021] Even though the metal covered area 5 on the interposer 4 could provide the capacitor plate directly, i.e. instead of providing the capacitor plate by means of conductive glue 3, this is less desirable.

[0022] There are several reasons for this. Using a non-conductive glue between the chip 1 and the metal covered area 5, increases the thickness of the dielectric insulating material between the capacitor plates and thus decreases the capacitance value for the capacitor  $C_5$  thus formed. Further the thickness of the glue will be much less well defined than the thickness of the insulating layer 2, such as a silicon dioxide layer, on the chip, which, due to the precision in the manufacturing process for the chip 1, may be made very thin and well defined.

[0023] The capacitance value has been found to be approximately ten times higher when using conductive glue as compared to non-conductive glue.

[0024] Thus without the conductive glue 3 the capacitance value becomes both smaller and less predictable.

[0025] The vias 7 form a conducting member which connects the second capacitor plate to an exterior ground node according to the invention.

[0026] Though each via 7 at the frequencies of interest only exhibits a relatively small impedance, in the applications of the invention having a large number of vias 7 coupled in parallel in order to lower the impedance further over a range of frequencies is important.

**[0027]** Thus, in order to have as many vias 7 as possible and the best possible electrical connection from the glue to the vias, a large metal covered area, preferably formed integrally with the vias 7 is desirable.

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**[0028]** It is known that any conducting member exhibits an inductance. Thus, an LC series circuit is formed by the capacitance provided between internal parts of the chip and the conductive glue 3 separated by the dielectric layer 2, and the inductance provided by the vias 7. If the chip has a well defined working frequency, the number of vias may be chosen, so that the series resonant frequency of the inductance provided by the vias and the aforementioned capacitance, approximately matches the working frequency of the chip. In this way an extremely low ground impedance of 2 Ohms or less, can be achieved.

**[0029]** It should be noted that the vias 7 in the preferred embodiment are not connected in parallel directly on the supporting interposer 4. Instead they are, as shown in Fig. 1, connected in parallel via the conductive paths 16 on the printed circuit board 10 on which the chip package, containing the chip 1 and interposer 4 assembly according to the invention, is eventually mounted.

**[0030]** This illustrates one way of connecting the vias 7 in parallel, and numerous other ways may be devised by the skilled person.

**[0031]** In particular it should be noted, that the resonant frequency of the ground plane is influenced by the number of vias 7 actually connected in parallel for a given application, and by the way this is done, as well as by the inductance of the die and the layout of the PCB 10.

**[0032]** Further, as shown in Fig. 1, a number of DC ground paths may be provided.

**[0033]** A ground pad 13 is connected to a via 6 through a bonding wire 8 which in turn is connected to the PCB ground plane 12 by via 14. The impedance of this path is essentially inductive at the frequencies of interest.

**[0034]** Another ground pad 15 is connected to conducting member 11 on interposer 4 through bonding wire 9 which is connected to the PCB ground plane 12 by vias 7. Either, or both, of the above described DC ground paths may be used. It should be noted that most circuits require at least one DC ground path.

**[0035]** The DC ground paths may also be used for AC signals if very low ground impedance is not required.

**[0036]** The components in Fig. 2 are identified by the same reference numerals as used in Fig. 1. Thus  $L_8$  is the inductance of the bonding wire 8,  $L_{14}$  the inductance of the via 14,  $C_5$  the capacitance between internal parts of the chip 1 and the capacitor plate provided by the glue 3,  $L_9$  the inductance of bondwire 9,  $L_{11}$  the inductance of conducting member 11 on interposer 4, and  $L_7$  the combined inductance of the vias 7, when they are eventually connected in parallel.

**[0037]** Fig. 4 illustrates the difference between the impedance to ground when an AC-ground plane according to the invention is used (line 20), and when only the inductive DC ground is used (line 22). Both axes are logarithmic. In particular the dip in impedance at  $f_0$  should be noted, since at this specific frequency the impedance of the ground path becomes virtually zero. Thus if this frequency  $f_0$  matches the operating frequency of the chip, a very low impedance ground path is provided for the chip. However, even if  $f_0$  is not tuned to the working frequency of the circuit, the ground impedance obtained by using the AC-



ground plane is still much lower with the invention than without the invention when working frequency of the circuit is greater than  $f_a$

**[0038]** It has been found that using the an AC-ground plane according to the invention there may be provided a substantial noise reduction at desired frequencies.

[ What is claimed is: